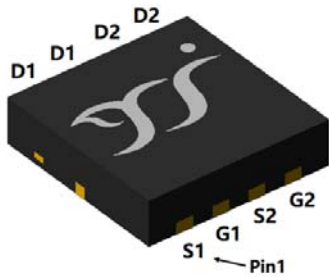
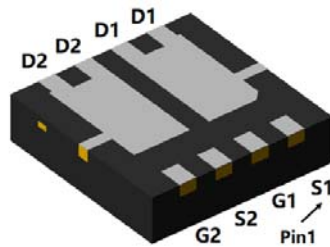


## N-Channel and P-Channel Complementary MOSFET



Top View



Bottom View

### Product Summary

#### NMOS

- $V_{DS}$  40V
- $I_D$  24A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ )  $<16m\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ )  $<21m\Omega$

#### PMOS

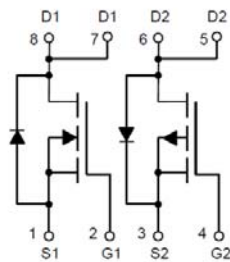
- $V_{DS}$  -40V
- $I_D$  -18A
- $R_{DS(ON)}$ ( at  $V_{GS}=-10V$ )  $<29m\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ )  $<41m\Omega$
- 100% EAS Tested

### General Description

- Trench Power LV MOSFET technology
- High density cell design for low  $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Wireless charger
- Load switching
- Power management



DFN3333-8L

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		$V_{DS}$	40	-40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	7	-5	A
	$T_A=100^\circ C$		4	-3	
	$T_C=25^\circ C$		24	-18	
	$T_C=100^\circ C$		15	-11	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	96	-72	A
Avalanche energy <sup>B</sup>		EAS	6.25	6.25	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	1.6	1.6	W
	$T_A=100^\circ C$		0.6	0.6	
	$T_C=25^\circ C$		18.9	19.5	
	$T_C=100^\circ C$		7.5	7.8	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient	Steady-State	$R_{\theta JA}$	60	75	60	75	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	5.5	6.6	5.3	6.4	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ016NP04A	F1	Q016NP04A	5000	10000	100000	13" reel



# YJQ016NP04A

## ■ NMOS Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.0	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	-	11.5	16	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	-	15	21	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =15A, V <sub>GS</sub> =0V	-	-	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	3	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	24	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz	-	965	-	pF
Output Capacitance	C <sub>oss</sub>		-	96	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	85	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =15A	-	21.4	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.4	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	5	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =15A, di/dt=100A/us	-	6.3	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	11.7	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =15A R <sub>GEN</sub> =2.2Ω	-	7.8	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	143	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	25.6	-	
Turn-off fall Time	t <sub>f</sub>		-	5.2	-	



# YJQ016NP04A

## ■ PMOS Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V	-	-	-1	μA
		V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	-100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.1	-1.6	-2.1	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A	-	22	29	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-8A	-	30	41	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-15A, V <sub>GS</sub> =0V	-	-	-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	16	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	-18	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, f=1MHz	-	1225	-	pF
Output Capacitance	C <sub>oss</sub>		-	120	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	110	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-15A	-	27	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.5	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	4.2	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-15A, di/dt=100A/us	-	20	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	21	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-20V, I <sub>D</sub> =-15A R <sub>GEN</sub> =2.2Ω	-	7.7	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	106.7	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	68.3	-	
Turn-off fall Time	t <sub>f</sub>		-	37.6	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. NMOS: T<sub>J</sub>=25°C, V<sub>GS</sub>=10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=5A.  
PMOS: T<sub>J</sub>=25°C, V<sub>GS</sub>=-10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=-5A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on the 40mm\*40mm\*1.1mm FR-4 PCB board with 1 in<sup>2</sup> pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



# YJQ016NP04A

## ■ NMOS Typical Electrical and Thermal Characteristics Diagrams

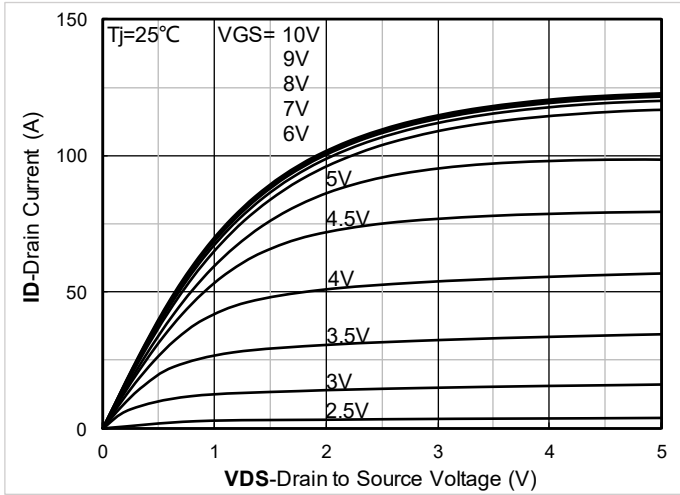


Figure 1. Output Characteristics

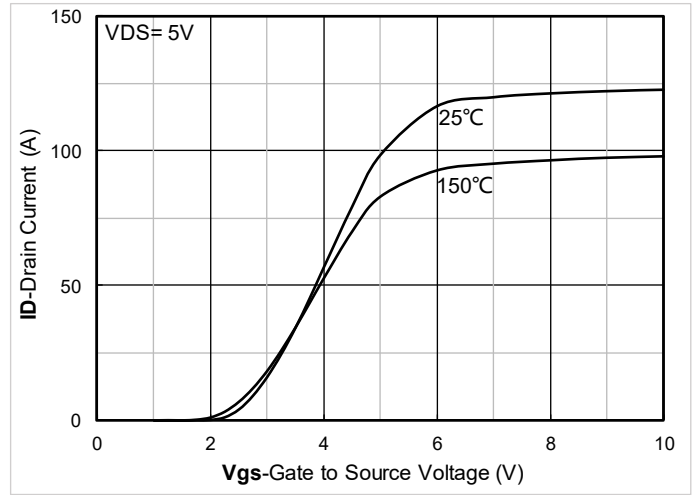


Figure 2. Transfer Characteristics

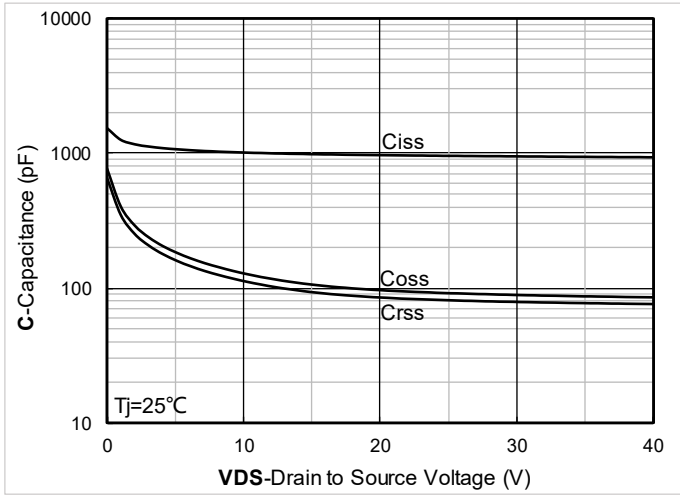


Figure 3. Capacitance Characteristics

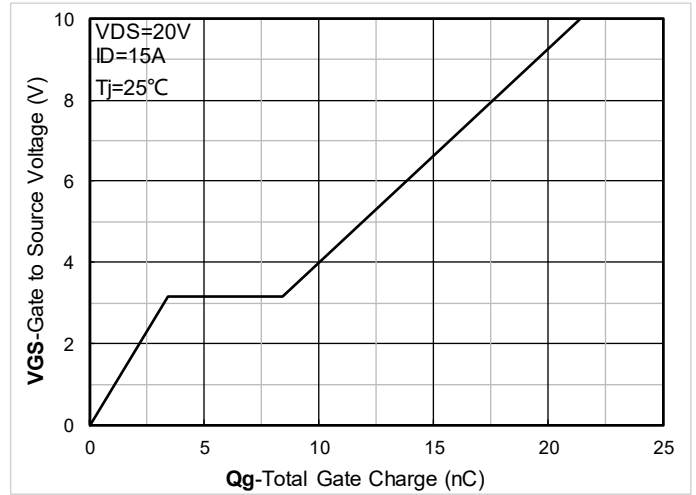


Figure 4. Gate Charge

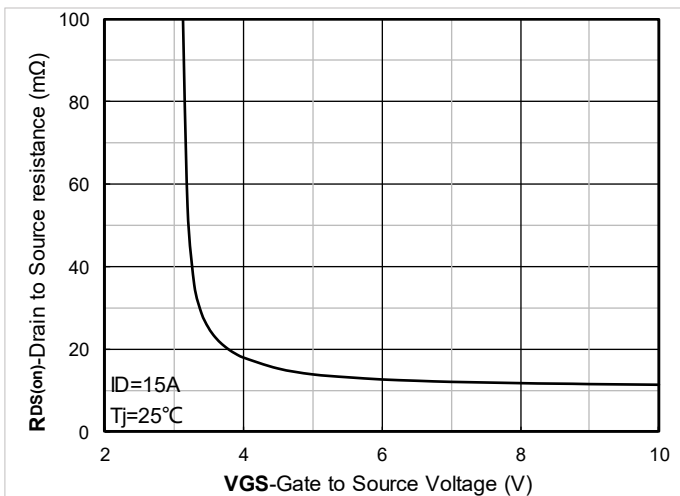


Figure 5. On-Resistance VS Gate to Source Voltage

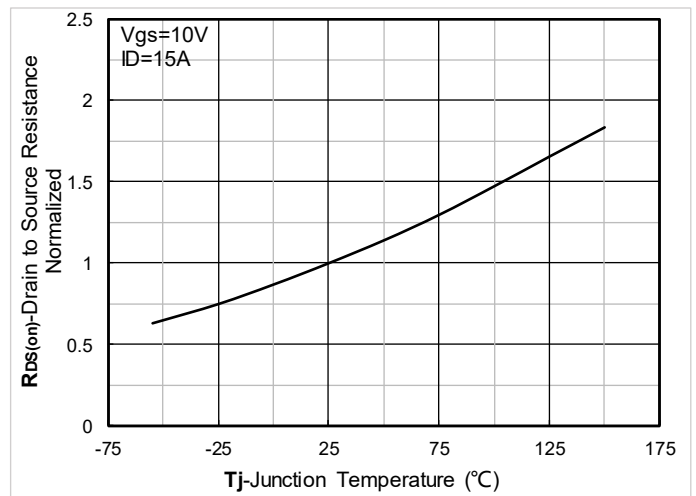


Figure 6. Normalized On- Resistance



# YJQ016NP04A

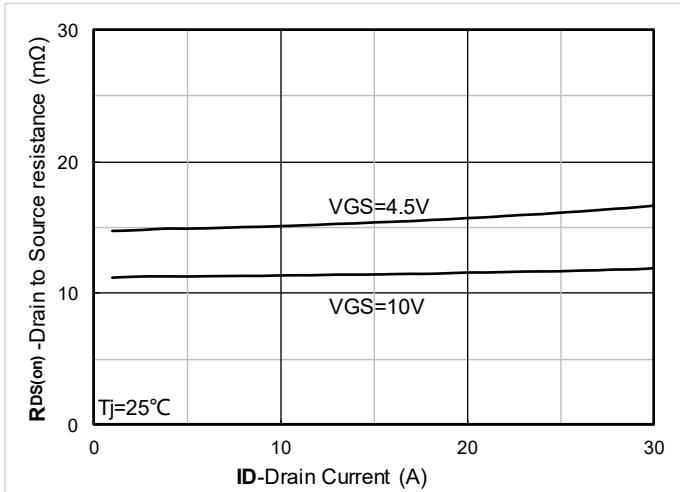


Figure 7.  $R_{DS(on)}$  VS Drain Current

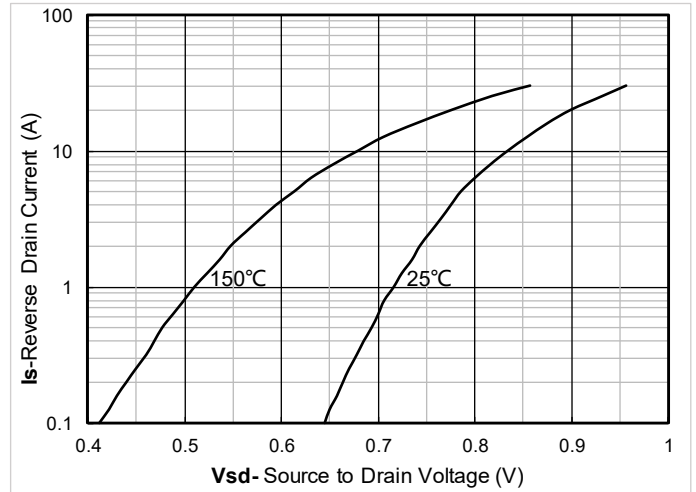


Figure 8. Forward characteristics of reverse diode

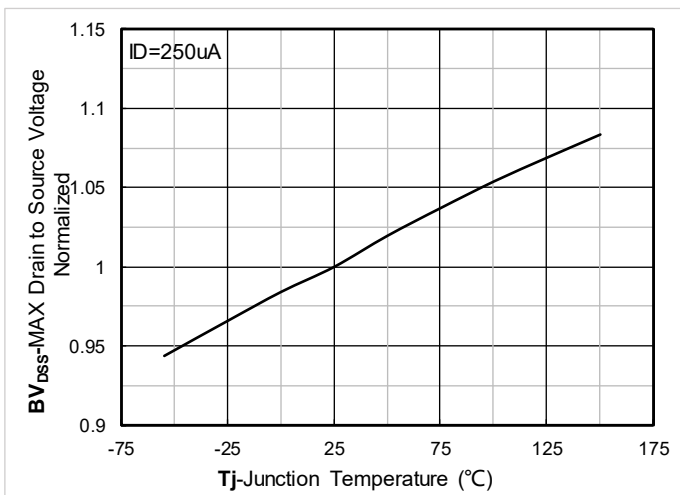


Figure 9. Normalized breakdown voltage

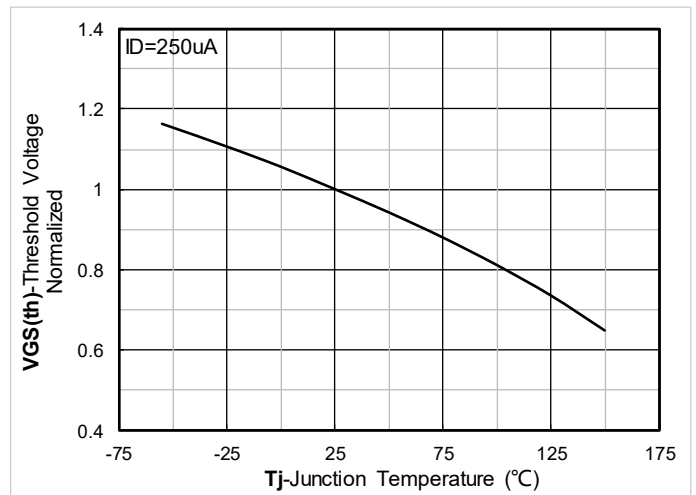


Figure 10. Normalized Threshold voltage

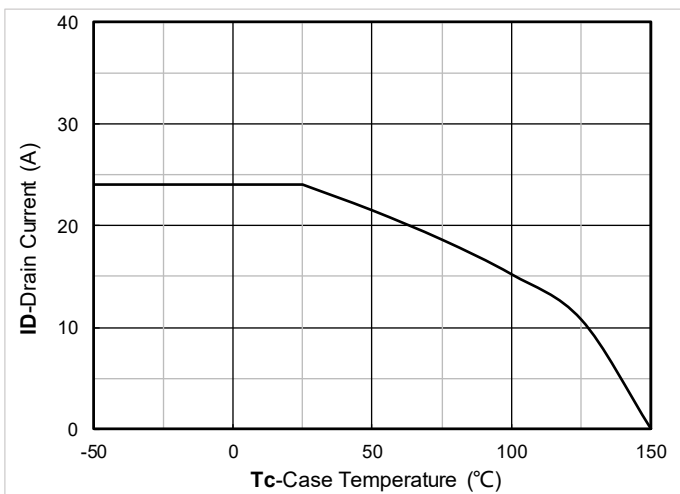


Figure 11. Current dissipation

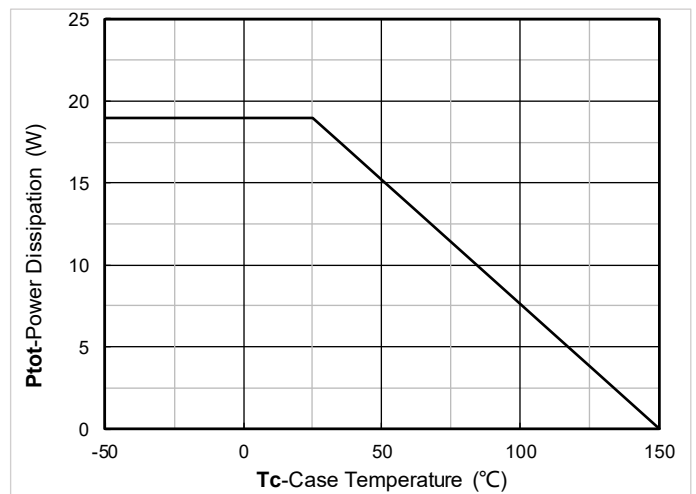


Figure 12. Power dissipation



# YJQ016NP04A

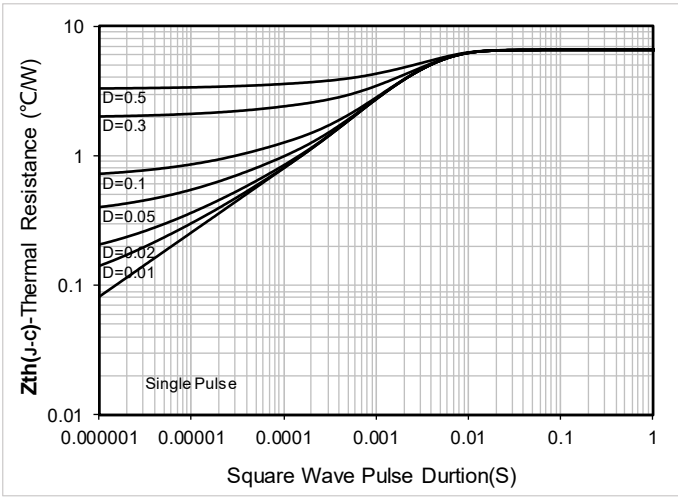


Figure 13. Maximum Transient Thermal Impedance

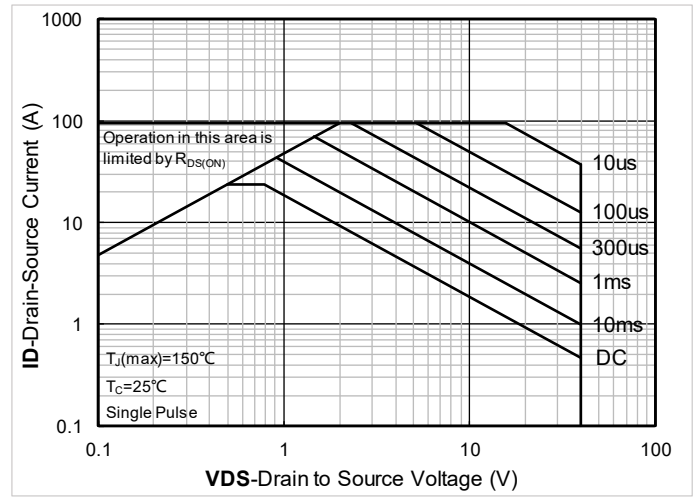


Figure 14. Safe Operation Area

## PMOS Typical Electrical and Thermal Characteristics Diagrams

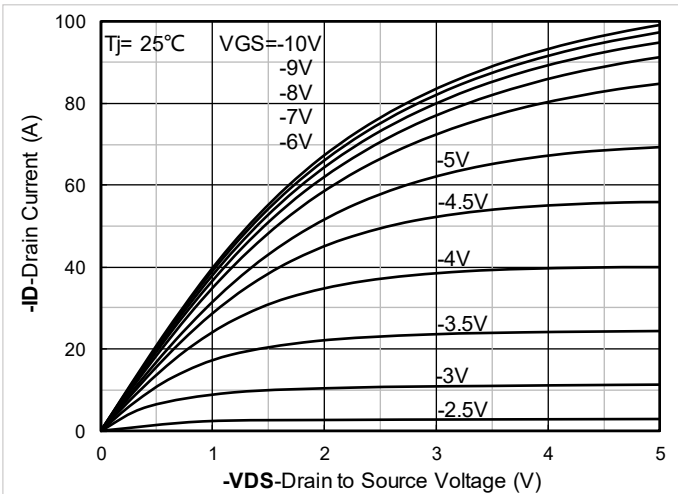


Figure 1. Output Characteristics

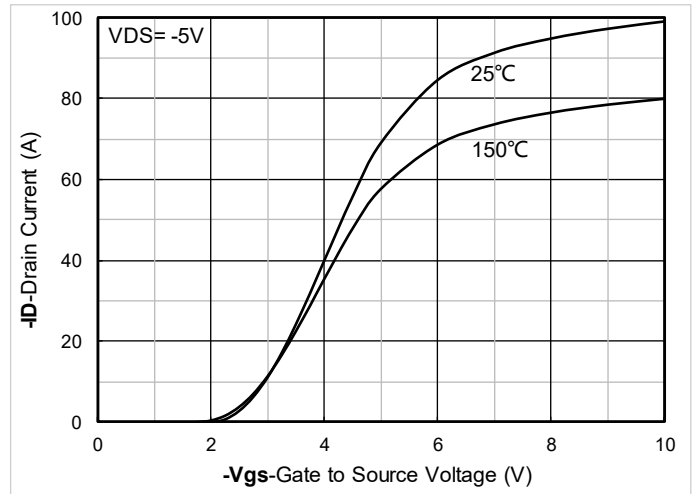


Figure 2. Transfer Characteristics

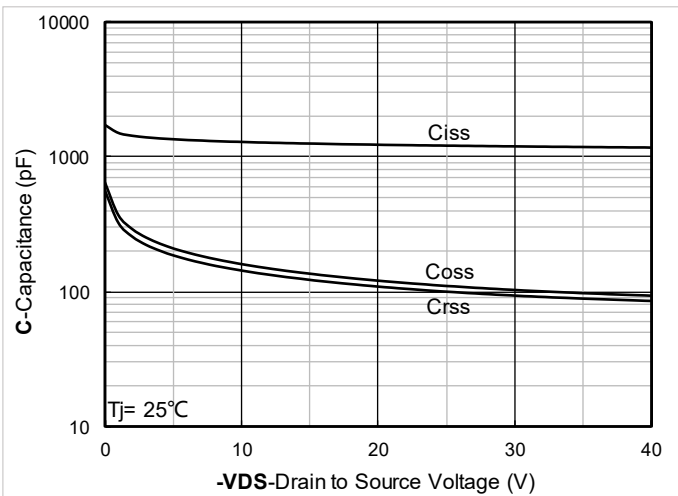


Figure 3. Capacitance Characteristics

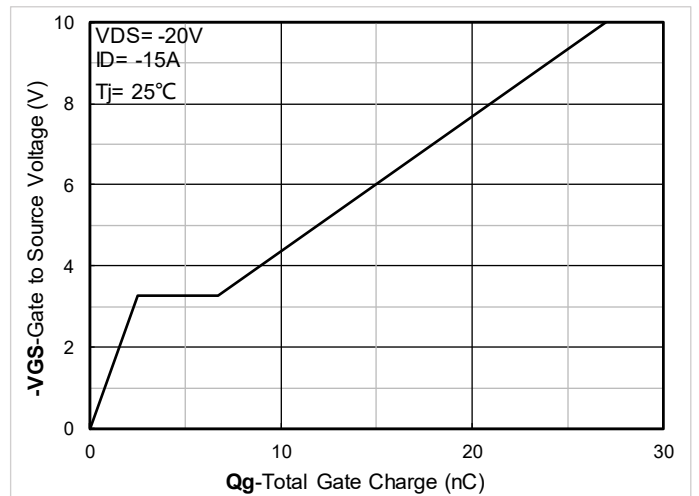


Figure 4. Gate Charge



# YJQ016NP04A

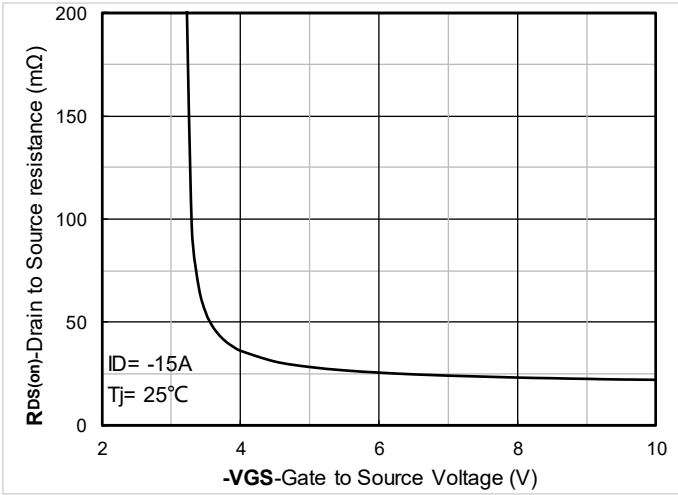


Figure 5. On-Resistance vs Gate to Source Voltage

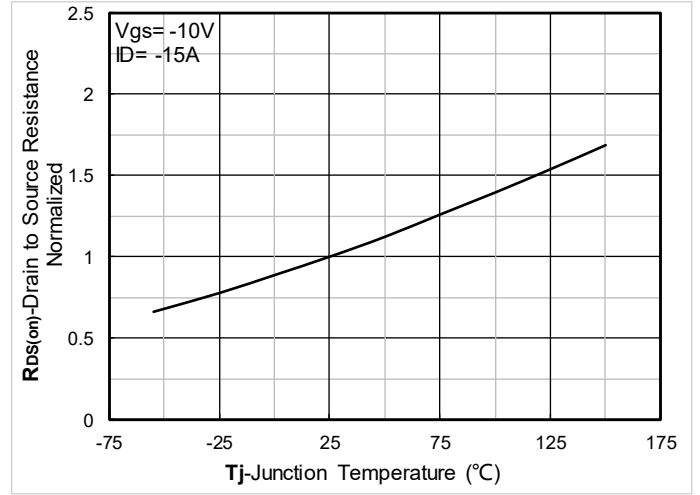


Figure 6. Normalized On-Resistance

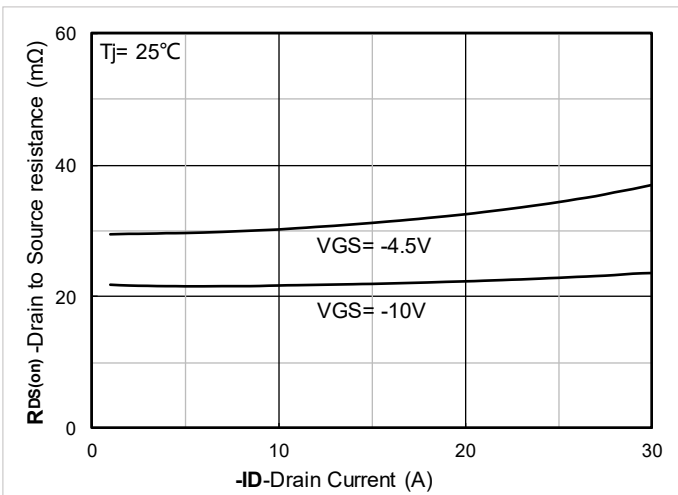


Figure 7. RDS(on) VS Drain Current

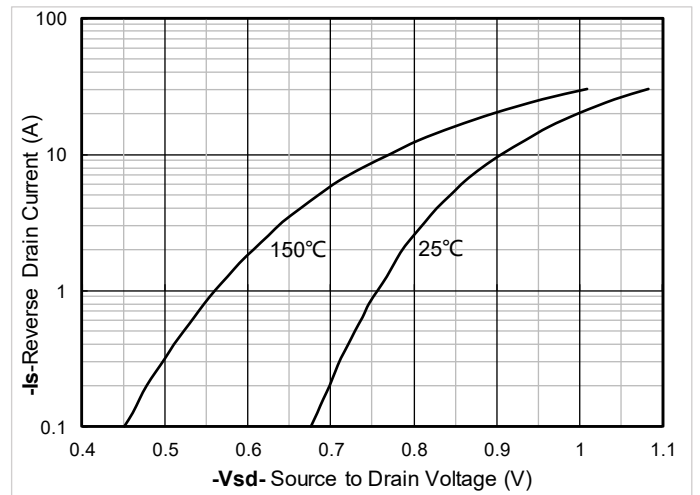


Figure 8. Forward characteristics of reverse diode

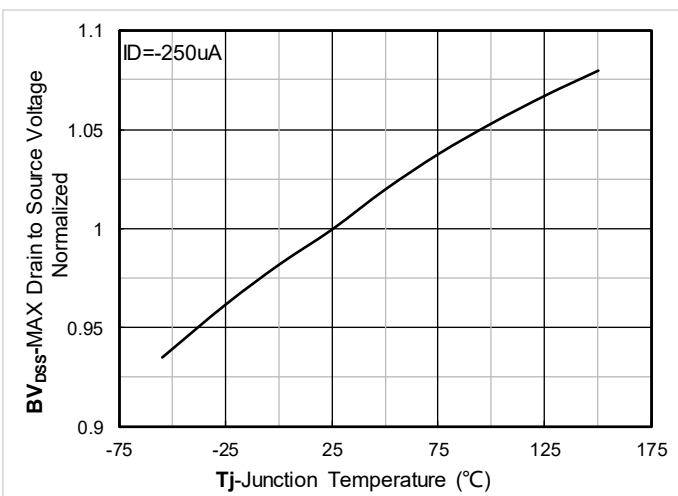


Figure 9. Normalized breakdown voltage

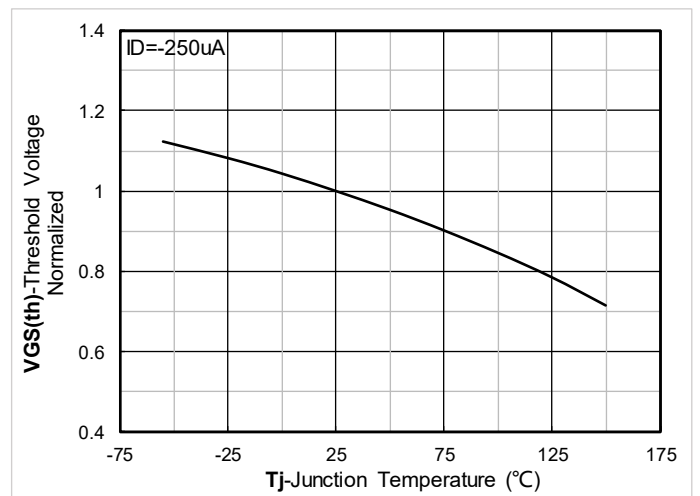


Figure 10. Normalized Threshold voltage



# YJQ016NP04A

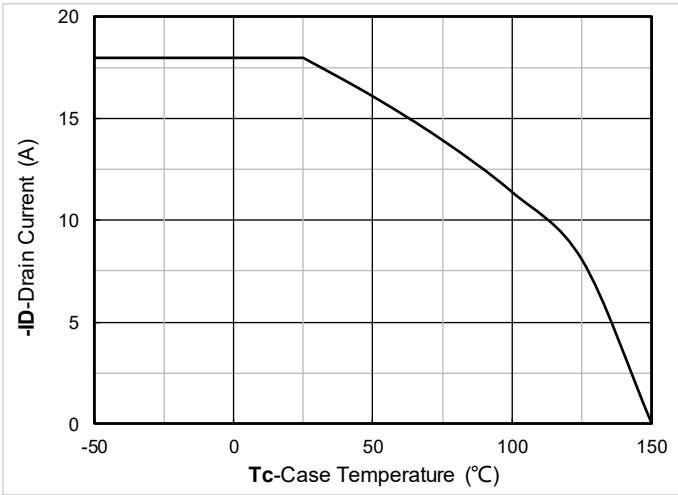


Figure 11. Current dissipation

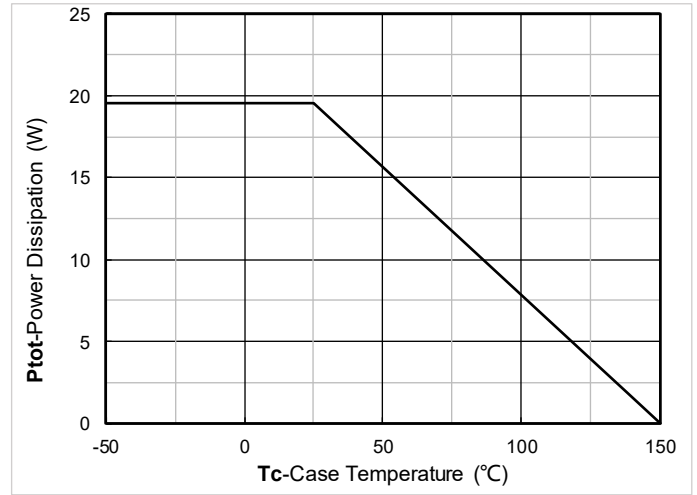


Figure 12. Power dissipation

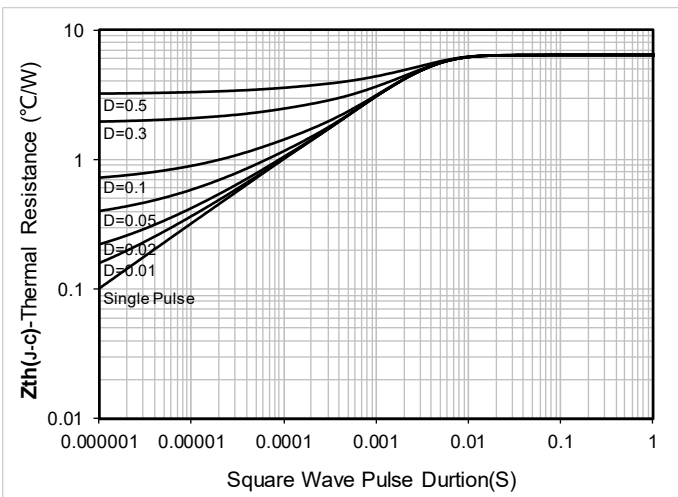


Figure 13. Maximum Transient Thermal Impedance

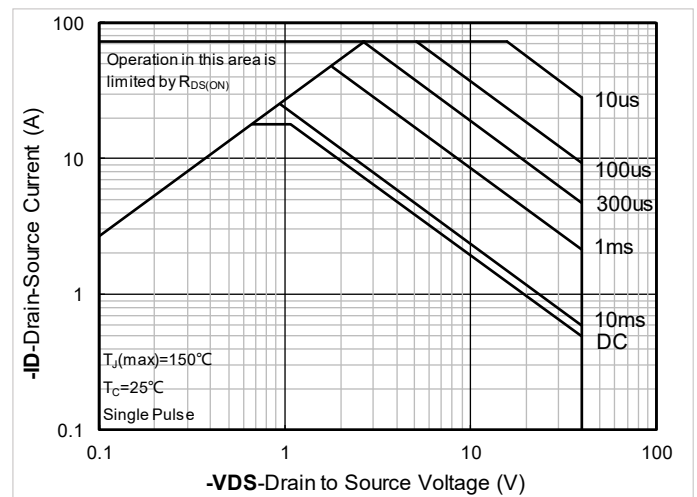


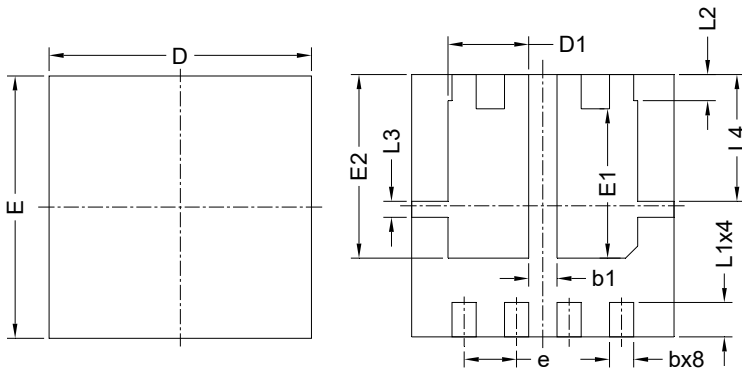
Figure 14. Safe Operation Area





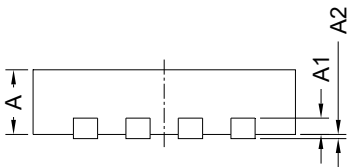
# YJQ016NP04A

## ■ DFN3333-8L-B-0.8MM Package information

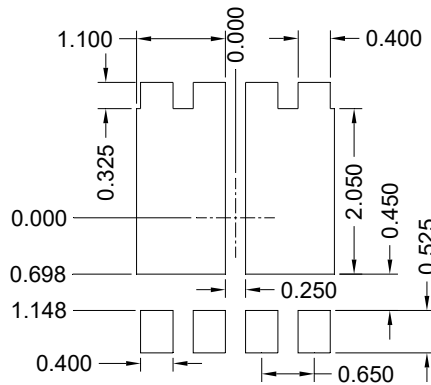


Top View  
正面视图

Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
E2	2.175	2.275	2.375
L1	0.325	0.425	0.525
L2	0.325 BSC		
L3	0.200 BSC		
L4	1.570 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		
b1	0.35 REF		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



# YJQ016NP04A

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